REMARKS:

Claims 4-7 and 11 have been amended and claim 22 has been added herein. Upon entry of this amendment, claims 1-13 and 15-22 will be pending in the above-identified Application.

Claims 4-7 and 9

Applicants respectfully request reconsideration of the rejection of claims 4-7 and 9 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,246,070 (Yamazaki) in view of U.S. Patent No. 6,265,730 (Nakanishi). As amended claims 4-7 and 9 recite forming a protective insulating film directly on and in physical contact with said first layer without using an etching process, the protective insulating film having a thickness of about 100 nm.

Yamazaki discloses an insulating film 105 having a thickness within the range of 5 nm to 50 nm, with a preference for being between 10 nm to 20 nm (column 8, lines 31-35). Nakanishi discloses a thin-film transistor having a gate insulating film. Yamazaki does not show or suggest having a protective insulating film directly on and in physical contact with said first layer without using an etching process, the protective insulating film having a thickness of about 100 nm.

As amended, claim 6 further recites that, in the laminate forming step, the precursor layer for an active layer is formed on the gate insulating film, the precursor layer is crystallized to form an active layer, and then the protective insulating film is formed on the active layer. Yamazaki discloses forming insulating film 105 on initial semiconductor film 104 (column 7, lines 8-10) and *then* crystallizing the initial semiconductor film 104 to form a crystalline semiconductor film 106 (column 9, lines 27-31). Yamazaki and Nakanishi fail, individually and in combination, to show or suggest the precursor layer being crystallized to form an active layer and *then* the protective insulating film being formed on the active layer.

As amended, claim 5 further recites that the precursor layer comprises an amorphous silicon film and the active layer comprises a polysilicon film. Yamazaki discloses the initial semiconductor film 104 being crystallized into a crystalline

semiconductor, such as a polycrystal silicon film (column 9, lines 27-31). Yamazaki and Nakanishi, individually and in combination, fail to show or suggest a precursor layer comprising an amorphous silicon film and an active layer comprising a polysilicon film.

As amended, claim 9 further recites that, subsequent to the dopant implanting step, defects formed in the protective insulating film are recovered by applying a temperature of about 600 degrees Centigrade. Yamazaki discloses obtaining an activating effect of impurities in the source and drain regions and a restoring effect of the crystal structure of the active layer by thermal or laser annealing (column 11, lines 28-32). Yamazaki and Nakanishi do not show or suggest recovering defects formed in the protective insulating film by applying heat subsequent to the dopant implanting step. Further, Yamazaki and Nakanishi fail to disclose or suggest applying a temperature of 600 degrees Centigrade as claimed. The office action relies on In re Boesch, 617 F.2d 272 (CCPA 1980), in asserting that it would have been obvious to one of ordinary skill in the art to apply a temperature of 600 degrees Centigrade. The facts of the present application are distinguishable from the facts in Boesch. In Boesch, the prior art disclosed ranges that overlapped the range of the Boesch invention. See Boesch at 275-276. In the present case, Yamazaki and Nakanishi do not disclose ranges that include 600 degrees Centigrade regarding recovering defects from the protective insulating film.

Because Yamazaki and Nakanishi, individually or in combination, do not show or suggest every element of claims 4-7 and 9, the rejection is improper. Accordingly, Applicants request the rejection be withdrawn.

Claim 8

Applicants respectfully request reconsideration of the rejection of claim 8 under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki in view of Nakanishi, and further in view of U.S. Patent No. 6,063,654 (Ohtani). Claim 8 recites that the protective insulating film is formed on a surface of the amorphous silicon film by surface oxidation of the amorphous silicon film, and then the amorphous silicon film is

crystallized to form the polysilicon film, the surface oxidation comprising exposing the amorphous silicon film to hot steam of about 400 degrees Centigrade.

Yamazaki discloses plasma CVD and sputtering methods of forming the insulating film 105 (column 7, lines 10-15). Nakanishi discloses a thin-film transistor having a gate insulating film and an interlayer insulating film, but no protective insulating film. Ohtani discloses irradiating a surface of an amorphous silicon film 203 within an oxidizing atmosphere to form an oxide film. Yamazaki, Nakanishi, and Ohtani fail, individually or in combination to show or suggest a protective insulating film formed on a surface of the amorphous silicon film by surface oxidation of the amorphous silicon film, wherein the surface oxidation comprises exposing the amorphous silicon film to hot steam of about 400 degrees Centigrade. The office action relies on Boesch in asserting that it would have been obvious to form a protective insulating film on a surface of the amorphous silicon film by exposing the amorphous silicon film to hot steam of about 400 degrees Centigrade. The facts of the present application are distinguishable from the facts in Boesch. In Boesch, the prior art disclosed ranges that overlapped the range of the Boesch invention. See Boesch at 275-276. In the present case, Yamazaki, Nakanishi, and Ohtani fail to show or suggest ranges that include 400 degrees Centigrade regarding formation of a protective insulating film. Further, the rule of Boesch regarding the obviousness of discovering an optimum value of a variable is not directly applicable here because the variable at issue is the temperature of hot steam and hot steam is not disclosed or suggested in the references. In other words, discovering an optimum value for the temperature of hot steam variable would not have been obvious to a person practicing the Yamazaki invention because that variable was not present in Yamazaki.

Because the references fail, individually and in combination, to show or suggest all of the elements of the claim, the rejection is improper. Accordingly, Applicants respectfully request that the rejection be withdrawn.

Claim 11

Applicants respectfully request reconsideration of the rejection of claim 11 under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki in view of Nakanishi and further in view of U.S. Patent No. 6,281,552 (Kawasaki). As an initial matter, the rejection is improper because claim 11 depends from claim 4, which was improperly rejected as shown above. Claim 11 contains further patentable subject matter. As amended, claim 11 recites forming an interlayer insulating film directly on and in physical contact with the protective insulating film of the bottom-gate thin-film transistor, forming a planarizing layer directly on and in physical contact with the interlayer insulating film, forming a transparent electrode directly on and in physical contact with the planarizing layer, and forming an alignment layer directly on and in physical contact with the transparent electrode to comprise a TFT substrate.

Yamazaki and Nakanishi disclose TFT semiconductor devices. Kawasaki discloses an active matrix LCD device having an interlayer insulating film 151 formed directly on a protective insulating film 150 (Figs. 2B and 2C), transparent conductive film 603, and a liquid crystal 605 (column 14, lines 41-61). Kawasaki does not disclose or suggest forming an interlayer insulating film directly on and in physical contact with the protective insulating film of the bottom-gate thin-film transistor, forming a planarizing layer directly on and in physical contact with the interlayer insulating film, forming a transparent electrode directly on and in physical contact with the planarizing layer, and forming an alignment layer directly on and in physical contact with the transparent electrode to comprise a TFT substrate.

Because Yamazaki, Nakanishi, and Kawasaki, individually and in any combination, fail to show or suggest every element of the claim, the rejection is improper. Accordingly, Applicants request that the rejection be withdrawn.

Claim 15

Applicants respectfully request reconsideration of the rejection of claim 15 under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki in view of Nakanishi and further in view of U.S. Patent No. 6,420,758 (Nakajima) and U.S. Patent No.

6,582,837 (Toguchi). As an initial matter, the rejection is improper because claim 15 depends from claim 4, which was improperly rejected as shown above. Claim 15 contains further patentable subject matter. As amended, claim 15 recites a method of fabricating an organic EL device comprising forming the cathode layer, forming the electron-transporting layer, forming the luminescent layer, forming the hole-transporting layer, and forming the anode layer, *in this order.*

Yamazaki, Nakanishi, and Nakajima do not disclose the layers recited in claim 15. Toguchi discloses an organic EL device having an anode on a substrate, a hole-transporting layer on the anode, a luminescent layer on the hole-transporting layer, and a cathode on the luminescent layer (Fig. 3; col. 3 lines 8-12). Toguchi also discloses the same arrangement with an electron-transporting layer between the luminescent layer and the cathode (Fig. 2). Toguchi does not show or suggest forming the cathode layer, forming the electron-transporting layer, forming the luminescent layer, forming the hole-transporting layer, and forming the anode layer, *in this order.*

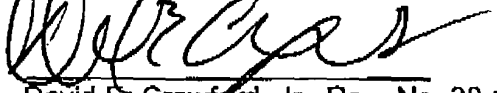
Because Yamazaki, Nakanishi, Nakajima, and Toguchi, individually or in any combination, do not show or suggest every element of claim 15, the rejection is improper. Accordingly, Applicants request the rejection be withdrawn.

Conclusion

As it is believed the Application is in condition for allowance, a favorable action and a Notice of Allowance are respectfully requested.

Dated: 13 JUL 04

Respectfully submitted,



David E. Crawford, Jr., Reg. No. 38,118
Customer No. 26263
314.259.5810